Modeling of Some Coplanar Waveguide Discontinuities

RAINEE N. SIMONS, MEMBER, 1EEE, AND GEORGE E. PONCHAK

Abstract — The paper presents lumped equivalent circuit models for several coplanar waveguide (CPW), discontinuities such as an open circuit, a series gap in the center conductor, and a symmetric step in the center conductor and gives their element values as a function of the discontinuity physical dimensions. The model element values are de-embedded from measured S parameters. In addition, the effects of the center conductor width and the substrate thickness on the equivalent circuit element values are presented. The characteristics of a CPW right angle bend employing a novel compensation technique is also presented. The frequency dependence of the effective dielectric constant is measured and compared to computed values.

I. Introduction

COPLANAR waveguide (CPW) on a dielectric substrate [1] consists of a center strip conductor with semi-infinite ground planes on either side (Fig. 1). This type of waveguide offers several advantages over conventional microstrip line: it facilitates easy shunt as well as series mounting of active and passive devices, it eliminates the need for wraparound and via holes, and it has a low radiation loss. These, as well as several other advantages, make CPW ideally suited for microwave integrated circuit applications [2], [3]. However, very little information is available in the literature on discontinuity models for CPW [4], [5]. This lack of sufficient discontinuity models for CPW has limited the application of CPW in microwave circuit design.

This paper presents for the very first time lumped-element equivalent circuit models for various CPW discontinuities together with their element values as a function of the discontinuity physical dimensions. These element values are de-embedded from measured scattering parameters of the discontinuities through a two-tier de-embedding technique. The discontinuities characterized in this paper are an open circuit, a series gap in the center conductor, and a symmetric step in the center conductor. These CPW circuits were fabricated on 0.125 in RT-5880 Duroid substrates. Second, the effect of the center conductor width on the CPW discontinuity equivalent circuit element values is investigated by characterizing a second set of 50 Ω circuits on Duroid substrates. Third, the effect of substrate thickness has been investigated by evaluating a set of discontinuity circuits fabricated on 0.062 in CuFlon substrates.

Manuscript received April 20, 1988; revised August 9, 1988. The authors are with the NASA Lewis Research Center, Cleveland, OH 44135.

IEEE Log Number 8824206.

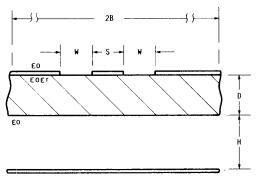


Fig. 1. Cross section of the coplanar waveguide in the test fixture.

Fourth, a simple technique to compensate for the difference in path length between the two slots of a CPW right angle bend is presented. Fifth, the frequency dependence of the effective dielectric constant, $\epsilon_{\rm eff}$, is measured using resonator techniques and compared to computed values from the literature. Last, the various sources of error and their effect on the de-embedded circuit element values are discussed.

II. De-Embedding Discontinuity Scattering Parameters

A. De-embedding Technique

Precision CPW calibration standards such as open circuits, short circuits, and 50 Ω matched loads for calibrating an automatic network analyzer (ANA) are not commercially available. Consequently, a two-tier deembedding technique which has been used successfully to characterize active devices such as GaAs MESFET's [6], [7] is used to characterize CPW discontinuities. The two-tier de-embedding technique consists of calibrating the ANA using precision coaxial standards and then using the calibrated ANA to characterize the test fixture. A CPW through line consisting of a uniform 50 Ω CPW line terminated at both ends by a linearly tapered CPW line which matches both the geometrical size and impedance of the 50 Ω CPW to a pair of coaxial connectors is placed in the test fixture during the fixture characterization. Thus, the CPW linear tapers, which are reproduced on all subsequent circuits by printed circuit board fabrication techniques, and the coaxial connectors form a part of the test fixture and are characterized initially.

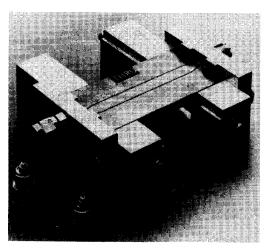


Fig. 2. Transition between a 50 Ω CPW and a coaxial connector using a linear taper transformer.

B. Coax-to-CPW Transition

The test fixture with the CPW through line on 0.125-in-thick Duroid is shown in Fig. 2. The lengths L and L_t of the uniform 50 Ω CPW line in the center and of each linear taper at the ends are 1.5 and 0.25 in, respectively. The coaxial connector used to excite the CPW is a modified SMA Hermetic Sparkplug Launcher (Dynawave Inc.) with pin and Teflon diameters of approximately 0.020 and 0.065 in, respectively. The center conductor width (S) and the slot width (W) of the uniform 50 Ω line are 0.178 and 0.010 in, respectively. The corresponding aspect ratio, S/(S+2W), is about 0.9. In order for this CPW line and the coaxial connector to be compatible, the width of the center conductor was tapered to about 0.045 in. The slot width remained 0.010 in. Thus the aspect ratio of the CPW at the coax launcher is about 0.69.

The characteristic impedance of the CPW with an aspect ratio of 0.69 is about 70 Ω . However, it provides a good impedance match to the 50 Ω coaxial line. The measured return loss is better than 16 dB over the frequency range of 0.045–18 GHz. The above discrepancy is in part due to the different definitions of characteristic impedance used for the CPW and the coaxial line. A similar discrepancy in impedance matching has been observed in the case of a microstrip line to slotline transition [8]. Linear tapers similar to the above are also fabricated for the second and third sets of circuits characterized on Duroid and CuFlon, respectively.

C. Equivalent Circuit Model for the Transition

A mixed lumped-distributed equivalent circuit topology to model the fixture is developed by taking into consideration the physical nature of the test fixture and the CPW circuit. The circuit model is shown in Fig. 3. The coaxial connectors are represented by a section of a lossy transmission line consisting of lumped elements in series with a small section of a coaxial line, L_c , for phase correction.

The tapered CPW section of length L_t is modeled as a multiple section stepped impedance transformer. EEsof Touchstone's [9] model of CPW as a lossless transmission line whose propagation characteristics are described by Ghione and Naldi [10] is used throughout the modeling experiment.

The elements of the equivalent circuit are then optimized over a 1 GHz band centered at 6 GHz to match the measured S parameters using the EEsof Touchstone circuit analysis and optimization programs. The circuit is first optimized using the random optimization routine. Then, the gradient optimizer is run until no further change in the equivalent circuit element values is seen. Fig. 4(a) and (b) shows the measured and modeled S_{11} and S_{21} characteristics for the test fixture and through line for the circuits on Duroid and CuFlon, respectively. This model is then used to de-embed the discontinuity characteristics from the fixture characteristics.

III. CPW OPEN CIRCUIT

A CPW open circuit is formed by ending the center conductor a short distance before the slot ends, thereby creating a gap, g_1 , as shown in Fig. 5. An electric field exists at the open circuit between the terminated center conductor and the surrounding ground conductor and hence gives rise to a capacitive reactance. This reactance is seen at a plane coincident with the open end of the center conductor. Thus the apparent position of the open circuit is beyond the physical end of the center conductor. The open circuit capacitance, C_{oc} , is a parallel combination of the capacitance due to the fringing fields across the gap, g_1 , and those across the slot, W. The gap-dependent capacitance varies proportionally as $1/g_1$. The slot-dependent capacitance is constant. Fig. 6(a) and (b) presents the de-embedded open circuit capacitance, C_{oc} , as a function of the open end gap width, g_1 , for circuits on Duroid and CuFlon substrates, respectively. C_{oc} saturates to a slotdependent capacitance for large values of g_1 . For two CPW lines with identical aspect ratios on the same substrate, C_{oc} is larger for the line with the wider center conductor.

IV. SERIES GAP IN THE CENTER CONDUCTOR

A series gap of length g in the center conductor of a CPW is shown in Fig. 5. The gap is modeled as a lumped Pi-network consisting of a coupling capacitance, C_2 , and two fringing capacitances, C_1 . In a way analogous to the open circuit, the capacitance across the gap, C_2 , decreases proportionally as 1/g. The fringing capacitance, C_1 , increases from the CPW line capacitance for g=0 to the open circuit saturation capacitance for large g. Fig. 7(a) and (b) presents the de-embedded capacitances as a function of the gap width, g, for circuits on Duroid and CuFlon substrates, respectively. C_1 and C_2 are larger for a 50 Ω line with a wider center conductor.

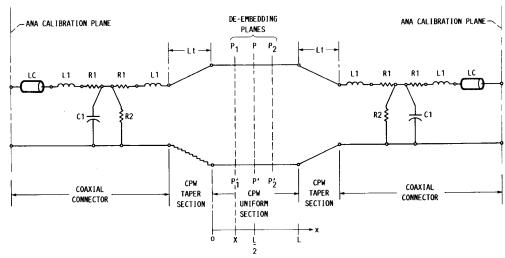


Fig. 3. A lumped equivalent circuit model of the transition between the 50 Ω CPW and coaxial line.

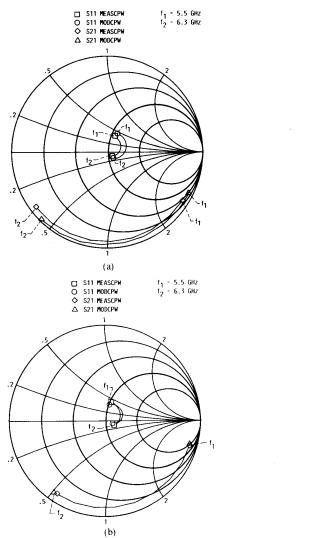


Fig. 4. Measured (MEASCPW) and modeled (MODCPW) S parameters of the transition between the CPW and coaxial line. (a) 0.125-in-thick Duroid. (b) 0.062-in-thick CuFlon.

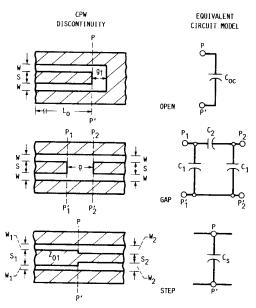


Fig. 5. Coplanar waveguide discontinuities and their lumped element equivalent circuit model.

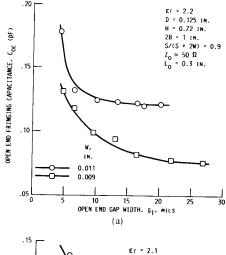
V. STEP CHANGE IN THE WIDTH OF CENTER CONDUCTOR

A step change in width of the center conductor of CPW is shown in Fig. 5. The step discontinuity perturbs the normal CPW electric and magnetic fields, which gives rise to additional reactances. These additional reactances are assumed to be lumped and located in the plane of the step discontinuity. The modeling experiments show that the reactances can be modeled as a shunt capacitance C_s . The influence of this capacitance is to effectively lengthen the lower impedance CPW line towards the higher impedance CPW line. Fig. 8(a) and (b) presents the de-embedded capacitance, C_s , as a function of the normalized step width for circuits on Duroid and CuFlon, respectively. As the normalized step change, S_1/S_2 , increases, C_s approaches the open-circuit saturation capacitance. For two lines with identical aspect ratios on the same substrate, C_s is larger for the line with the wider center conductor.

VI. RIGHT ANGLE BEND

A CPW right angle bend in which the width of the center conductor remains uniform is illustrated in Fig. 9. A right angle bend in a 50 Ω CPW line with a mean arm length L=1.0 in is fabricated on 0.125-in-thick Duroid and characterized in the fixture shown in Fig. 2. The measured S_{11} and S_{21} characteristics of the circuit are shown in Figs. 10(a) and 11(a), respectively. The poor return loss and large insertion loss are due to the phase distortion of the wavefront as it passes through the bend. The phase distortion is caused by the large difference in path length between the inner slot and the outer slot which guide the CPW mode.

One method to compensate for the difference in path length is to slow down the wave which travels in the inner



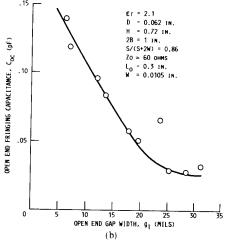


Fig. 6. Deembedded lumped fringing capacitance from measured *S* parameters as a function of the CPW open end gap width. (a) 0.125-in-thick Duroid. (b) 0.062-in-thick CuFlon.

slot so that it emerges from the bend in phase with the wave in the outer slot. A simple and practical technique to do this from a circuit fabrication point of view is to place a dielectric medium over the inner slot. This was done using a 0.5 in $\times 0.5$ in $\times 0.025$ in alumina slab as shown in Fig. 9. The measured S_{11} and S_{21} with the compensating dielectric slab are shown in Figs. 10(b) and 11(b), respectively. These figures show that the above technique is capable of proving compensation over a broad band.

VII. EFFECTIVE DIELECTRIC CONSTANT

The $\epsilon_{\rm eff}$ is determined from a pair of series-gap coupled straight resontators terminated in either an open circuit or a short circuit. The primary and higher order resonances for each resonator are used as outlined in [11]. Resonators are characterized for the following cases:

A. Resonator on 0.125-in-Thick Duroid Terminated in a Short Circuit

Fifty Ω transmission lines with two different center conductor widths but with identical aspect ratios, S/(S+

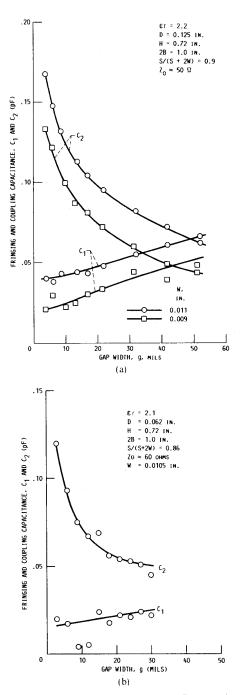
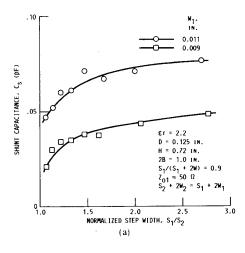


Fig. 7. Deembedded lumped fringing and coupling capacitances from measured S parameters as a function of the CPW gap width. (a) 0.125-in-thick Duroid. (b) 0.062-in-thick CuFlon.

2W) = 0.9, were used. Corresponding to each center conductor width, a pair of resonators are fabricated. Fig. 12(a) and (b) shows $\epsilon_{\rm eff}$ over the frequency range of 2–18 GHz for CPW lines with center conductor widths of 0.178 and 0.1454 in, respectively. Also shown in these figures are the computed $\epsilon_{\rm eff}$ using expressions in [1], [10], and [12]. Good agreement is observed between the experimentally deter-



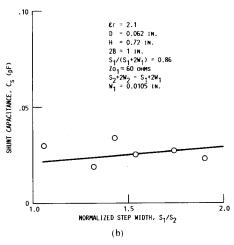


Fig. 8. Deembedded lumped shunt capacitance from measured S parameters as a function of the normalized CPW step width. (a) 0.125-in-thick Duroid. (b) 0.062-in-thick CuFlon.

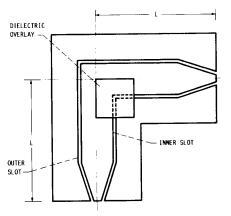


Fig. 9. Schematic illustrating a CPW right-angle bend with a dielectric overlay to compensate for the difference in path length between the inner and outer slots.

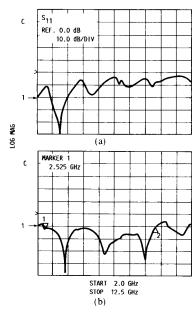


Fig. 10. Measured S_{11} of the CPW right-angle bend. (a) Uncompensated. (b) Compensated.

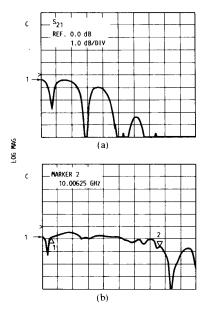


Fig. 11. Measured S_{21} of the CPW right-angle bend. (a) Uncompensated. (b) Compensated.

mined and computed $\epsilon_{\rm eff}$ using equations in [1] and [12] above 6 GHz. However, $\epsilon_{\rm eff}$ determined using equations in [10] are observed to be lower than the experimentally determined values.

The accuracy of $\epsilon_{\rm eff}$ derived from these resonators is questionable. The resonant frequency of the wavelengthlong resonator was lower than the resonant frequency of the half-wavelength-long resonator. This yields a line extension for the gap plus short circuit due to fringing fields which is negative. This is improbable. The reason for this

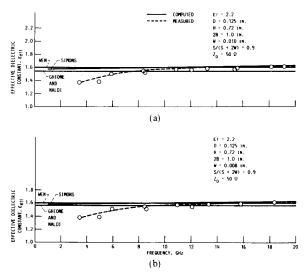


Fig. 12. Measured and computed effective dielectric constant for CPW as a function of frequency resonators on Duroid and terminated in a short circuit. (a) S = 0.178 in, W = 0.010 in, D = 0.125 in. (b) S = 0.1454 in, W = 0.008 in, D = 0.125 in.

is probably a fringing field for the short circuit which is dependent on the length of the CPW line. Preliminary results obtained for CPW short circuits using the two-tier de-embedding technique have shown this to be the case. Itoh [13] has also observed a similar behavior for microstrip resonators terminated in an open circuit. The dependence of the end effect length on the length of the resonator violates the assumption that the line extension is constant for both resonators and may therefore be subtracted.

B. Resonators on 0.125-in-Thick Duroid Terminated in an Open Circuit

Fig. 13(a) and 13(b) show $\epsilon_{\rm eff}$ determined with the resonators terminated in an open circuit. Good agreement is observed between experimentally determined and computed $\epsilon_{\rm eff}$ using equations in [12] over the entire frequency range. In this case, $\epsilon_{\rm eff}$ computed using equations in [10] is observed to be lower than the experimentally determined values across the entire band.

The open circuit terminated resonators yielded positive line extensions for the gap plus open circuit which agreed with the results in this paper. The difference between the $\epsilon_{\rm eff}$ obtained with resonators terminated in an open circuit and those terminated in a short circuit is greater for the lower order resonances. This is expected if the fringing field is not constant since lower order resonances are more susceptible to fringing field effects than higher order resonances.

C. Resonators on 0.062-in-Thick Cuflon Terminated in an Open Circuit

A 60 Ω CPW transmission line with an aspect ratio of 0.86 is used. Values for $\epsilon_{\rm eff}$ determined with a pair of resonators terminated in an open circuit are presented in

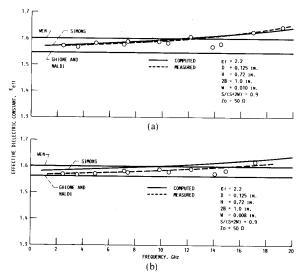


Fig. 13. Measured and computed effective dielectric constant for CPW as a function of frequency resonators on Duroid and terminated in an open circuit. (a) S = 0.178 in, W = 0.010 in, D = 0.125 in. (b) S = 0.1454 in, W = 0.008 in, D = 0.125 in.

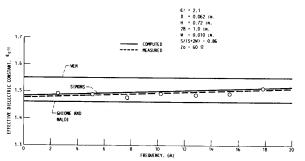


Fig. 14. Measured and computed effective dielectric constant for CPW as a function of frequency resonators on CuFlon and terminated in an open circuit. S = 0.123 in, W = 0.010 in, D = 0.062 in.

Fig. 14(a) and (b). In this case also, good agreement is observed between the experimentally determined and the computed $\epsilon_{\rm eff}$ using equations in [12] over the entire frequency range. Further, $\epsilon_{\rm eff}$ values determined using equations in [1] and [10] are observed to be higher and lower, respectively, than the experimentally determined value.

VIII. Errors and Their Effect on the De-embedded Parameters

In the experiment outlined in this paper, there are three basic sources which introduce error into the equivalent circuit element values: modeling errors, RF measurement errors, and geometrical errors. The modeling errors can be analyzed in two parts. The first part is due to the difference between the measured and modeled S-parameter characteristics of the coax-to-CPW transition model. Typically, this was about $\pm 3.3^{\circ}$ and $\pm 1.4^{\circ}$ for the circuits on Duroid and CuFlon, respectively. The second part is due to the difference between the experimentally determined

and computed $\epsilon_{\rm eff}$ used in the Touchstone program [9]. The Touchstone program uses the analytical expressions given in [10] for computing $\epsilon_{\rm eff}$. Since the value of $\epsilon_{\rm eff}$ predicted by [10] is lower than the experimentally determined values, a phase error is introduced in the equivalent circuit model. The phase error per transition model due to this is 1.82°, 0.77°, and 1.47° for the circuits used to characterize the transition in the three sets of circuits. These errors are regarded as systematic errors since they are constant throughout the experiment. The RF measurement errors are due to the nonrepeatability of the coax-to-CPW transition. Typically, the RF phase measurements are repeatable to $\pm 3^{\circ}$. The geometrical errors are due to variations in the processing of each circuit. Typically, the tolerance is ± 0.0001 in. These errors are regarded as random errors. The modeling routine repeatedly predicts the same value for the discontinuity equivalent circuit elements and therefore introduces minimal random errors.

A. Errors in Two-Port Circuits

The two-port characterization of the series gap in the center conductor and the step change in width of the center conductor are not susceptible to two of the above errors. They are geometrical errors along the length of the transmission line and errors due to the difference in $\epsilon_{\rm eff}$. The geometrical errors are minimized by designing the circuits to be reciprocal and using both the forward and reverse S parameters in the optimization routine. The optimization routine averages the forward and reverse characteristics and therefore minimizes these errors. All the two-port circuits were kept equal in length to the circuits used in the transition characterization. Hence, any differences between the computed and measured $\epsilon_{\rm eff}$ are compensated for in the transition model by the addition or subtraction of an equivalent length of transmission line.

B. Errors in One-Port Circuits

The one-port characterization of the open circuit is susceptible to all of the errors mentioned above. Therefore, a worst-case error estimate may be obtained by an analysis of how each affects $C_{\rm oc}$. $C_{\rm oc}$ can be approximated in terms of the equivalent end-effect length, I, as [11]

$$C_{\rm oc} \approx \frac{l\sqrt{\epsilon_{\rm eff}}}{(cZ_{\rm o})} = \frac{\beta 1}{\omega Z_{\rm o}} = \frac{\Delta \phi}{\omega Z_{\rm o}}$$
 (1)

where

c speed of light,

1 equivalent constant in CPW,

 β propagation constant in CPW,

 Z_0 characteristic impedance of the CPW,

ω angular frequency,

 $\Delta \phi$ phase in radians.

Using (1), the geometrical error introduces an uncertainty of ± 0.00021 pF in $C_{\rm oc}$. Similarly, the RF measurement error results in an uncertainty in $C_{\rm oc}$ of ± 0.0278 and ± 0.0232 pF for the circuits on Duroid and CuFlon, re-

spectively. Therefore, the maximum random error or spread in the data is ± 0.02801 and ± 0.02341 pF for the circuits on Duroid and CuFlon, respectively. The random errors cause the deviations in the data from the best fit curve drawn through the data.

The difference in the phase of the measured and modeled transition characteristics introduces an uncertainty in $C_{\rm oc}$ of ± 0.0306 and ± 0.0108 pF for the circuits fabricated on Duroid and CuFlon, respectively. Finally, the error created by the difference in $\epsilon_{\rm eff}$ needs to be analyzed. This is done by considering the coax-to-CPW transition model developed in Section II. In this model, the propagation constant, β_m , computed by Touchstone is lower than the measured propagation constant, β_a , as determined in Section VII. Therefore, an error of

$$\Delta \phi = (\beta_a - \beta_m)^* L \tag{2}$$

is created. One half of this error is compensated for in L_c of the lumped equivalent circuit model shown in Fig. 3. Thus, for a discontinuity located at an arbitrary plane P1-P1' which is at a distance X from the end of the taper as illustrated in Fig. 3, the error in the modeled circuit would be

$$\Delta \phi = (\beta_a - \beta_m) * \left(X - \frac{L}{2} \right). \tag{3}$$

Therefore a circuit connected to the transition by a length of line equal to L/2 would give the correct results. In the CPW open circuit investigated in Section III, X is 0.050 in. Therefore, the following errors in $C_{\rm oc}$ are found: $C_{\rm oc} = -0.0157$ pF for the CPW line with S = 0.178 in $C_{\rm oc} = -0.0066$ pF for the CPW line with S = 0.1454 in, and $C_{\rm oc} = -0.0106$ pF for the CPW line with S = 0.123 in. This error can be subtracted from the reported results since the sign of the error term is known.

IX. CONCLUSIONS

The paper presents for the very first time lumped equivalent circuit models for the following CPW discontinuities: an open circuit, a series gap in the center conductor, and a symmetric step in the center conductor. The model element values are de-embedded from measured S parameters using a two-tier de-embedding technique and are presented as a function of the discontinuity physical dimensions. The effects of the center conductor width and the substrate thickness on the equivalent circuit element values are also presented. A new technique to compensate for the difference in path length between the two slots of a CPW right angle bend has been demonstrated. The frequency dependence of $\epsilon_{\rm eff}$ is measured and compared with computed results from the literature. The various sources of error and their effect on the de-embedded results are discussed.

REFERENCES

 C. P. Wen, "Coplanar waveguide: A surface strip transmission line suitable for nonreciprocal gyromagnetic device applications," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-17, pp. 1087–1090, Dec. 1969.

- [2] R. E. Stegens and D. N. Alliss, "Coplanar microwave integrated circuit for integrated subsystems," *Microwave Syst. News and Commun. Tech.*, vol. 17, pp. 84–96, Oct. 1987.
- [3] D. Neuf and S. Spohrer, "Ultrasmall MIC mixer designed for ECM applications," Microwave Syst. News and Commun. Tech., vol. 15, pp. 70-80, Oct. 1985.
- [4] K. C. Gupta, R. Garg, and R. Chadha, Computer-aided Design of Microwave Circuits. Dedham, MA: Artech House, 1981, chap. 6.
- [5] R. K. Hoffmann, Handbook of Microwave Integrated Circuits. Norwood, MA: Artech House, 1987, chap. 13.
- [6] R. Lane, "Deembedding device scattering parameters," *Microwave J.*, vol. 27, pp. 149-156, Aug. 1984.
 [7] G. E. Elmore and L. J. Salz, "Quality microwave measurement of
- [7] G. E. Elmore and L. J. Salz, "Quality microwave measurement of packaged active devices," *Hewlett - Packard J.*, vol. 38, pp. 39-48, Feb. 1987.
- [8] S. B. Cohn, "Slot-line on a dielectric substrate," IEEE Trans. Microwave Theory Tech., vol. MTT-17, pp. 768-778, Oct. 1969.
- [9] EEsof Touchstone Reference Manual, version 1.5, EEsof Inc., Mar. 1987.
- [10] G. Ghione and C. Naldi, "Analytical formulas for coplanar lines in hybrid and monolithic MICs," *Electron. Lett.*, vol. 20, pp. 179–181, Feb. 1984.
- [11] T. C. Edwards, Foundations for Microstrip Circuit Design. New York: Wiley, 1981, chaps. 5 and 7.
- [12] R. N. Simons, "Suspended coupled slotline using double layer dielectric," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-29, pp. 162–165, Feb. 1981.
- [13] T. Itoh, "Analysis of microstrip resonators," IEEE Trans. Microwave Theory Tech., vol. MTT-22, pp. 946-952, Nov. 1971.

¥



Rainee N. Simons (S'76-M'80) received the B.E. degree in electronics and communications from the Mysore University in 1972, the M. Tech. degree in electronics and communications from the Indian Institute of Technology, Kharagpur, in 1974, and the Ph.D. degree in electrical engineering from the Indian Institute of Technology, New Delhi, in 1983.

He is currently a Resident Research Associate in the Solid State Technology Branch of the Space Electronics Division, NASA Lewis Re-

search Center, Cleveland, OH. From 1985 to 1987 he was a National Research Council Research Associate and carried out investigations on the direct optical control of GaAs microwave semiconductor devices and circuits. Prior to this, he was a Senior Scientific Officer at the Indian Institute of Technology, New Delhi, and worked on fin-line components for mm-wave applications and also on toroidal latching ferrite phase shifters for phased arrays. His current research interests include analysis and modeling of GaAs microwave semiconductor devices and circuits in MMIC's, optical control, and high temperature superconductivity.

Dr. Simons held the post of IEEE Student Chapter Chairman at the Indian Institute of Technology, New Delhi, from 1978 to 1979. He also held the post of IEEE Indian Council Ed/MTT Society Chapter (New Delhi) Joint Secretary, Executive Committee Member, and Vice Chairman during the years 1982, 1983, and 1984, respectively.

¥



George E. Ponchak received his BEE from Cleveland, State University, Cleveland, OH, in 1983 and the M.S.E.E. from Case Western Reserve University, Cleveland, OH, in 1986. He joined the NASA Lewis Research Center, Cleveland, OH, in July 1983 as a member of the Space Communications Division. Since joining NASA he has been engaged in research in solid-state technology development, transmission lines, and monolithic microwave integrated circuits (MMIC's).